LISTING OF THE CLAIMS

A detailed listing of claims is presented below. Please amend currently amended claims as indicated below including substituting clean versions for pending claims with the same number. In addition, clean text versions of pending claims not being currently amended that are under examination are also presented. It is understood that any claim presented in a clean version below has not been changed relative to the immediate prior version.

1. (Currently Amended) A method of automatically detecting memory size comprising the steps of:

a) sending a READ command from a memory controller chip to a serial peripheral interface (SPI) device over an SPI interface for a first series of eight serial clock cycles;

b) driving a data Input/Output (D-IO) pin in said memory controller chip low for a second series of eight serial clock cycles;

c) floating said D-IO pin <u>after said second series of eight serial clock cycles, such that said D-IO pin is weakly pulled down in the absence of data from said SPI device and is overcome in the presence of data from said SPI device</u>;

d) automatically determining that said SPI device has memory addresses of up to nine bits when detecting the presence of a first non-zero value coming from said SPI device through said D-IO pin during a third series of eight serial clock cycles; and

e) automatically determining that said SPI device has memory addresses of up to sixteen bits when detecting the presence of a first zero value at said D-IO pin during said third series of eight serial clock cycles and a second non-zero value coming from said SPI device through said D-IO pin during a fourth series of eight serial clock cycles.

2. (Previously Presented) A method as described in Claim 1, wherein said SPI device having memory addresses of up to nine bits is an EEPROM having up to five hundred twelve (512) bytes of memory.

3. (Previously Presented) A method as described in Claim 1, wherein said SPI device having memory addresses of up to sixteen bits is an EEPROM having up to 64 kilobytes of memory.

4. (Original) A method as described in Claim 1, wherein steps d) and e) are performed by a sensing circuit located within said memory controller chip.

5. (Original) A method as described in Claim 1, wherein said memory controller chip drives a serial clock signal between said memory controller chip and said SPI device.

6. (Original) A method as described in Claim 1, wherein said SPI device has a non-zero value located at its first address byte.

7. (Previously Presented) A method as described in Claim 1, wherein said SPI interface uses three controller pins at said memory controller chip including a serial clock pin, a chip select pin, and said D-IO pin that is coupled to a serial input (SI) and serial output (SO) pin on said SPI device, said SI and SO pins coupled to form a bi-directional signal, said SI and SO pins also coupled to a pulldown resistor, said pulldown resistor pulling down said D-IO pin in order to float said D-IO pin to a logic "0" level as described in step c).

8. (Original) A method as described in Claim 1, wherein zero values for said third and fourth series of eight serial clock cycles indicate the absence of said SPI device.

9. (Previously Presented) A method as described in Claim 1, wherein said SPI device having larger memory is detected comprising the further step of:

automatically detecting the presence of said first zero value at said D-IO pin during said third series of eight serial clock cycles, a second zero value at said D-IO pin during said fourth series of eight serial clock cycles, and a third non-zero value coming from said SPI device through said D-IO pin during a fifth series of eight serial clock cycles with said sensing circuit indicating that said SPI device memory addresses of up to twenty-four bits.

10. (Original) A method as described in Claim 1, wherein step c) further comprises pulling down said D-IO pin, that is floated, to a logic "0" level with a pulldown resistor, said pulldown resistor coupled to said D-IO pin, a serial input (SI) pin, and a serial output (SO) pin of said SPI device.

11. (Original) A serial peripheral interface (SPI) circuit for automatically detecting memory size comprising:

a memory controller chip comprising a first serial clock pin for providing a clock signal, a data Input/Output (D-IO) pin, and a first chip select pin for sending a chip select signal;

an SPI device comprising a second serial clock pin for receiving said clock signal, a serial input pin (SI) coupled to a serial output (SO) pin, and a second chip select pin for receiving said chip select signal;

a pulldown resistor coupled to said SI and SO pins;

a sensing circuit for detecting data signals coming from said SPI device;

means for coupling said SPI device to said memory controller chip, said sensing circuit, and to said pulldown resistor; and

means for detecting memory size of said SPI device.

12. (Original) An SPI interface circuit as described in Claim 11, wherein said means for coupling comprises:

means for coupling said first and second serial clock pins;

means for coupling said D-IO pin to said SI pin, to said SO pin, and to said pulldown resistor; and

means for coupling said first and second chip select pins.

13. (Original) An SPI interface circuit as described in Claim 11 further comprising:

means for coupling said SI and SO pins to form a single bi-directional signal; and

means for coupling said SI and SO pins to said pulldown resistor.

14. (Currently Amended) An SPI interface circuit as described in Claim 11, wherein said means for detection comprises:

a) means for sending a READ command from said memory controller chip to said SPI device over said SPI interface circuit for a first series of eight serial clock cycles;

b) means for driving said data Input/Output (D-IO) pin in said memory controller chip low for a second series of eight serial clock cycles;

c) means for floating said D-IO pin and weakly pulling down said D-IO pin with said pulldown resistor to a logic "0" level after said second series of eight

<ins>clock cycles, such that the D-IO pin is weakly pulled down in the absence of data from the SPI device and is overcome with the presence of data from the SPI device;</ins>

d) means for automatically determining that said SPI device has memory addresses of up to nine bits when detecting the presence of a first non-zero value coming from said SPI device through said D-IO pin during a third series of eight serial clock cycles with said sensing circuit; and

e) means for automatically determining that said SPI device has memory addresses of up to sixteen bits when detecting the presence of a first zero value during said third series of eight serial clock cycles with said sensing circuit.

15. (Previously Presented) An SPI interface circuit as described in Claim 11, wherein said means for detection comprises:

a) means for sending a READ command from said memory controller chip to said serial peripheral interface (SPI) device over said SPI interface circuit for a first series of eight serial clock cycles;

b) means for driving said data Input/Output (D-IO) pin in said memory controller chip low for a second series of eight serial clock cycles;

c) means for floating said D-IO pin and weakly pulling down said D-IO pin with said pulldown resistor to a logic "0" level;

d) means for automatically determining that said SPI device has memory addresses of up to nine bits when detecting the presence of a first non-zero value coming from said SPI device through said D-IO pin during a third series of eight serial clock cycles with said sensing circuit;

e) means for automatically determining that said SPI device has memory addresses of up to sixteen bits when detecting the presence of a first zero value coming from said SPI device through said D-IO pin during said third series of eight serial clock cycles with said sensing circuit and a second non-zero value coming

from said SPI device through said D-IO pin during a fourth series of eight serial clock cycles with said sensing circuit; and

f) means for automatically determining that said SPI device has memory addresses of up to twenty-four bits when detecting the presence of said first zero value coming from said SPI device through said D-IO pin during said third series of eight serial clock cycles, a second zero value during a fourth series of eight serial clock cycles, and a third non-zero value coming from said SPI device through said D-IO pin during a fifth series of eight serial clock cycles with said sensing circuit.

16. (Original) An SPI interface circuit as described in Claim 11, wherein said SPI device has a non-zero value located at its first address byte.

17. (Original) An SPI interface circuit as described in Claim 11, wherein zero values for said third, fourth, and fifth series of eight serial clock cycles indicate the absence of said SPI device, wherein said memory controller chip instructs a USB chip coupled to said memory controller chip to enumerate using internal values.

18. (Currently Amended) A system comprising a processor and a memory unit, wherein said memory unit contains instructions that when executed implement a method of automatically detecting memory size comprising the steps of:

a) sending a READ command from a memory controller chip to a serial peripheral interface (SPI) device over an SPI interface for a first series of eight serial clock cycles;

b) driving a data Input/Output (D-IO) pin in said memory controller chip low for a second series of eight serial clock cycles;

c) floating said D-IO pin after said second series of eight serial clock cycles, such that said D-IO pin is weakly pulled down in the absence of data from said SPI device and is overcome in the presence of data from said SPI device;

d) automatically determining that said SPI device has memory addresses of up to nine bits when detecting the presence of a first non-zero value coming from said SPI device through said D-IO pin during a third series of eight serial clock cycles; and

e) automatically determining that said SPI device has memory addresses of up to sixteen bits when detecting the presence of a first zero value at said D-IO pin during said third series of eight serial clock cycles, and a second non-zero value coming from said SPI device through said D-IO pin during a fourth series of eight serial clock cycles.

19. (Previously Presented) A system as described in Claim 18, wherein said SPI device having memory addresses of up to nine bits is an EEPROM having up to five hundred twelve (512) bytes of memory.

20. (Previously Presented) A system as described in Claim 18, wherein said SPI device having memory addresses of up to sixteen bits is an EEPROM having up to 64 kilobytes of memory.

21. (Original) A system as described in Claim 18, wherein steps d) and e) are performed by a sensing circuit located within said memory controller chip.

22. (Original) A system as described in Claim 18, wherein said memory controller chip drives a serial clock signal between said memory controller chip and said SPI device.

23. (Original) A system as described in Claim 18, wherein said SPI device has a non-zero value located at its first address byte.

24. (Previously Presented) A system as described in Claim 18, wherein said SPI interface uses three controller pins at said memory controller chip including a serial clock pin, a chip select pin, and said D-IO pin that is coupled to a serial input (SI) and serial output (SO) pin on said SPI device, said SI and SO pins coupled to form a bi-directional signal, said SI and SO pins also coupled to a pulldown resistor, said pulldown resistor pulling down said D-IO pin in order to float said D-IO pin to a logic "0" level as described in step c).

25. (Original) A system as described in Claim 18, wherein zero values for said third and fourth series of eight serial clock cycles indicate the absence of said SPI device.

26. (Previously Presented) A system as described in Claim 18, wherein said SPI device having larger memory is detected comprising the further step of:

automatically detecting the presence of said first zero value at said D-IO pin during said third series of eight serial clock cycles, a second zero value at said D-IO pin during said fourth series of eight serial clock cycles, and a third non-zero value coming from said SPI device through said D-IO pin during a fifth series of eight serial clock cycles with said sensing circuit indicating that said SPI device memory addresses of up to twenty-four bits.

27. (Original) A system as described in Claim 18, wherein step c) further comprises pulling down said D-IO pin, that is floated, to a logic "0" level with a

pulldown resistor, said pulldown resistor coupled to said D-IO pin, a serial input (SI) pin, and a serial output (SO) pin of said SPI device.